Amendments to the Drawings:

The attached drawing sheet includes changes to figure 1. This sheet replaces the original sheet including figure 1.

REMARKS

Claims 1-9 are presented for reconsideration and further examination in view of the foregoing amendments and following remarks.

In the outstanding Office Action, the Examiner rejected claims 1 – 9 under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement; and rejected claims 1 – 4 and 9 under 35 U.S.C. §103(a) as being unpatentable over the admitted prior art (hereinafter, "AAPA") in view of U.S. Patent No. 5,388,022 to Ahuja (hereinafter, "Ahuja"). The Examiner noted that claims 5 – 8 would be allowable if rewritten in independent form and to overcome the rejection under 35 U.S.C. §112. By this Response and Amendment, claims 1 – 3 have been amended and the rejections thereto and to the claims dependent thereon have been traversed.

Support for the amendments to claims 1 – 3 can be found in the specification as originally filed. It is respectfully submitted that the above amendments introduce no new matter within the meaning of 35 U.S.C. § 132.

Objection to the Drawings

In the outstanding Office Action, the Examiner objected to the drawings because figure 1 lacked an appropriate legend designating that it illustrates only prior art.

Response

By this Response and Amendment, Applicant submits a replacement sheet of drawings which adds the label "prior art" to figure 1.

Accordingly, Applicant respectfully requests that the Examiner withdraw the objection to the drawings.

Rejection Under 35 U.S.C. §112

The Examiner rejected claims 1 –9 under 35 U.S.C. §112, first paragraph, for failing to comply with the written description requirement.

Response

By this Response and Amendment, Applicant respectfully traverses the Examiner's rejection.

Claims 1 and 2 have been amended to remove the term "onset" objected to by the examiner, and now recite residual current detection circuits wherein, *inter alia*, "first and second signals [are] applied to a circuit stage" and wherein "the application of the second signal to the circuit stage is delayed with respect to the application of the first signal to the circuit stage." (Present Application, Claims 1 and 2, emphasis added). Consequential amendments have been made to claim 3. This change is fully supported by the specification – see, for example, page 6, lines 20-23 which clearly refer to the voltage applied at the second input terminal being delayed compared to that applied at the first input terminal, it being understood, of course, that the voltages referred to in that passage are the first and second signals generically referred to in claims 1 and 2 (see also page 3, lines 30-32).

Applicant submits that all of the features of amended independent claims 1 and 2, and of claims 3 – 9 which depend from them, are sufficiently supported by the specification.

Accordingly, Applicant respectfully requests that the Examiner reconsider and withdraw the rejection to claims 1 – 9 under 35 U.S.C. §112.

Rejection Under 35 U.S.C. §103(a)

The Examiner rejected claims 1 – 4 and 9 under 35 U.S.C. §103(a) as being unpatentable over AAPA in view of Ahuja.

Response

By this Response and Amendment, Applicant respectfully traverses the Examiner's rejection since the cited prior art does not disclose, teach or suggest all of the features of the presently claimed invention.

To establish a *prima facie* case of obviousness, the Examiner must establish: (1) some suggestion or motivation to modify the references exists; (2) a reasonable expectation of success; and (3) the prior art references teach or suggest all of the claim limitations. *Amgen, Inc. v. Chugai Pharm. Co.*, 18 USPQ2d 1016, 1023 (Fed. Cir. 1991); *In re Fine,* 5 USPQ2d 1596, 1598 (Fed. Cir. 1988); *In re Wilson*, 165 USPQ 494, 496 (CCPA 1970).

Claim 1 recites a residual current detection circuit including, *inter alia*, "a circuit stage which produces an output only when the applied first and second signals are coincident." Claim 2 recites "a circuit stage for providing an output signal only when the applied first and second signals are coincident."

AAPA discloses a residual current detection circuit; however, it does not disclose, teach, or suggest a circuit breaker with an AND gate that is able to output a signal when simultaneous signals are present. Ahuja discloses an auto-reset circuit breaker in which the solid state switch 16 opens if *either one* of two negative-going signals, as shown in Figures 1(c) and 1(d), is present at the input of gate 30. Gate 30 operates as an OR gate (and not an AND gate) with respect to its input signals, and therefore Ahuja does not disclose, teach, or suggest a circuit breaker with an AND gate that is able to output a signal when simultaneous signals are present. Further, neither AAPA nor Ahuja discloses, teaches, or suggests a first output channel which provides a first signal "while the amplitude of the output exceeds a predetermined level."

Applicant understands from paragraph 10 (Response to Arguments) of the outstanding Office

Action that the Examiner interprets the "onset" of the first and second signals - now referred to as the *application* of the first and second signals to the circuit stage - as the logic 0 to logic 1 transitions in the waveforms of Figures 1(c) and 1(d) of Ahuja. Applicant concedes that on that interpretation the second signal is indeed delayed relative to the first. However, the meaningful signals in Ahuja are not the logic 1 regions of the waveforms but the logic zero regions – see col. 3, lines 53-56 where it is explained that it is the low-going control signal shown in Figure 1(c) which is produced by the overcurrent condition and which trips the switch 16. Accordingly, the first and second signals of Ahuja which ought, in the Examiner's analysis, to be taken as analogous to the first and second signals of claim 1 are the logic zero regions of the waveforms of Figures 1(c) and 1(d) respectively of Ahuja. However, as explained above and in our previous response, in Ahuja these signals are not ANDed but ORed, since the presence of either one is sufficient to trip the switch 16. Further, the two signals are applied to the AND gate 30 at the same time, and it is only the positive-going trailing edge of the second signal (Figure 1(d)) which is delayed.

Accordingly, if this principle were applied to the residual current detector of AAPA, the result would be that a "trip" signal would be generated immediately by the negative-going leading edge of the first signal (Figure 1(c)), and maintained beyond the positive-going trailing edge of the latter until the delayed positive-going trailing edge of the second signal (Figure 1(d)). This is precisely the opposite of the function sought to be achieved by the present invention, where an immediate response is not required. Accordingly, the Ahuja circuit, if used in AAPA, would do nothing to mitigate the incidence of nuisance tripping and in fact would tend to exacerbate the situation by prolonging the response period.

In order to avoid misinterpretations of the above type, Applicant has amended claims 1 and 2 to specify that the first signal is provided "*while* the amplitude of the output exceeds a predetermined

level" (Emphasis added). The output referred to is, of course, the output corresponding in amplitude to the magnitude of the residual current. The basis for this amendment is to be found, inter alia, at page 6, lines 8-18, where it is explained that the FWR output voltage is fed directly to a first input terminal of the AND gate, i.e. without delay, but that an input signal to the AND gate will only be produced when the voltage exceeds the threshold associated with the input terminal. The same distinction has been made at line 7 of claim 2 by changing "when" to "while".

By this amendment it is made clear that the first signal is a signal coincident with an undesirably high residual current, as determined (in the embodiment) by the threshold of the AND gate input terminal. The corresponding signal in Ahuja is the logic zero region of the waveform at Figures 1(c), since this is what is produced in coincidence with an undesirable overcurrent condition for which tripping of the switch 16 is required. Therefore, in combining the disclosures of AAPA and Ahuja, applicant submits that the Examiner can only reasonably compare the first and second signals of claim 1 with the logic zero regions of the waveforms at Figures 1(c) and 1(d). As already shown, the logic zero regions of Ahuja are not applied at different times to the AND gate and, since they are logic zero, they are ORed rather than ANDed. Accordingly, for this reason and those given above, claims 1 and 2 could not be rendered obvious by AAPA in view of Ahuja.

As claims 3 – 9 depend from amended claim 2, Applicant submits that these claims too are not rendered obvious by AAPA in view of Ahuja.

Accordingly, Applicant respectfully requests that the Examiner reconsider and withdraw the outstanding rejections to these claims.

Allowable subject matter

The Examiner objected to claims 4 – 8 as dependent from rejected base claim 2, but indicated

that claims 4 and 5 would be allowable if rewritten in independent form.

Response

As applicant submits that claim 2 is now in condition for allowance, applicant requests that the Examiner reconsider and withdraw the objections to claims 4 – 8, which depend from claim 2.

CONCLUSION

In light of the foregoing, Applicant submits that the application is now in condition for allowance. If the Examiner believes the application is not in condition for allowance, Applicant respectfully requests that the Examiner contact the undersigned attorney if it is believed that such contact will expedite the prosecution of the application.

In the event this paper is not timely filed, Applicant petitions for an appropriate extension of time. Please charge any fee deficiency or credit any overpayment to Deposit Account No. 14-0112.

Respectfully submitted,

NATH & ASSOCIATES PLLC

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APPENDIX